PATENT ABSTRACTS OF JAPAN

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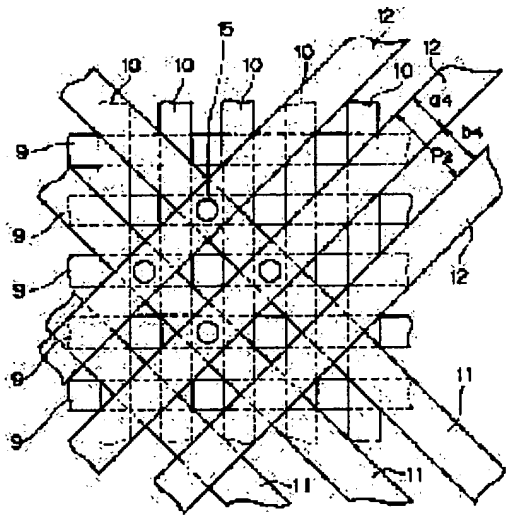
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a technique for manufacturing a semiconductor integrated circuit device which is high in performance and capable of being easily manufactured.

SOLUTION: A semiconductor integrated circuit device is equipped with a first wiring layer 9 and a second wiring layer 10 which cross each other at right angles and a third wiring layer 11 and a fourth wiring layer 12 which intersect each other at right angles. At this point, the wiring layers 9 and 10 are equal to each other in wiring pitch, and the wiring layers 11 and 12 are equal to each other in wiring pitch, and the wiring pitch of the wiring layers 11 and 12 is 21/2 times as large as that of the wiring layers 9 and 10.



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CLAIMS

[Claim(s)]
[Claim 1] It is semiconductor integrated circuit equipment which the wiring layer of the 1st layer and the wiring layer of a two-layer eye lie at right angles in the wiring layer of semiconductor integrated circuit equipment, and the wiring layer of the 3rd layer and the wiring layer of the 4th layer lie at right angles, and is characterized by arranging said wiring layer of the 3rd layer with whenever [tilt-angle / of about 45 degrees] to the wiring layer of said two-layer eye.
[Claim 2] In semiconductor integrated circuit equipment according to claim 1, the wiring pitch of the wiring layer of the 1st layer and the wiring pitch of the wiring layer of a two-layer eye are equal. For the wiring pitch of the wiring layer of the 3rd layer, and the wiring pitch of the wiring layer of the 4th layer, it is equal and the wiring pitch of said wiring layer of the 3rd layer and said wiring layer of the 4th layer is 21/2 of the wiring pitches of said wiring layer of the 1st layer, and the wiring layer of said two-layer eye. Semiconductor integrated circuit equipment characterized by being twice.
[Claim 3] It is semiconductor integrated circuit equipment which sets to semiconductor integrated circuit equipment according to claim 1 or 2, and is characterized by the center line of two or more wiring layers of the 3rd layer and two or more wiring layers of the 4th layer passing along the midpoint of the adjoining crossing in each crossing with the center line of two or more wiring layers of the center line of two or more wiring layers of the 1st layer, and a two-layer eye.
[Claim 4] The wiring layer for connection holes prepared in semiconductor integrated circuit equipment given in any 1 term of claims 1-3 between the wiring layer of said two-layer eye, said wiring layer of the 3rd layer and said wiring layers of the 4th layer, and those lower layer wiring layers is semiconductor integrated circuit equipment characterized by being the pillar of a column configuration.
[Claim 5] The process which forms the wiring layer of the 1st layer on the base with which two or more semiconductor devices are formed, The process which arranges and forms the wiring layer of a two-layer eye through an interlayer insulation film on said wiring layer of the 1st layer so that it may intersect perpendicularly to said wiring layer of the 1st layer, The process which arranges and forms the wiring layer of the 3rd layer through an interlayer insulation film on the wiring layer of said two-layer eye so that whenever [tilt-angle] may turn into 45 degrees to the wiring layer of said two-layer eye, The manufacture approach of semiconductor integrated circuit equipment of having the process which arranges and forms the wiring layer of the 4th layer through an interlayer insulation film on said wiring layer of the 3rd layer so that it may intersect perpendicularly to said wiring layer of the 3rd layer.
[Claim 6] In the manufacture approach of semiconductor integrated circuit equipment according to claim 5, the wiring pitch of the wiring layer of the 1st layer and the wiring pitch of the wiring layer of a two-layer eye are equal. The wiring pitch of the wiring layer of the 3rd layer and the wiring pitch of the wiring layer of the 4th layer are equal. The wiring pitch of said wiring layer of the 3rd layer, and said wiring layer of the 4th layer 21/2 of the wiring pitches of said wiring layer of the 1st layer, and the wiring layer of said two-layer eye The manufacture approach of the semiconductor integrated circuit equipment characterized by being twice.
[Claim 7] It is the manufacture approach of the semiconductor integrated circuit equipment which sets to

the manufacture approach of semiconductor integrated circuit equipment according to claim 5 or 6, and is characterized by the center line of two or more wiring layers of the 3rd layer and two or more wiring layers of the 4th layer passing along the midpoint of the adjoining crossing in each crossing with the center line of two or more wiring layers of the center line of two or more wiring layers of the 1st layer, and a two-layer eye.

[Claim 8] It is the manufacture approach of the semiconductor integrated circuit equipment characterized by arranging partially said wiring layer of the 3rd layer, or said wiring layer of the 4th layer to said wiring layer of the 1st layer, or the wiring layer of said two-layer eye in the manufacture approach of semiconductor integrated circuit equipment given in any 1 term of claims 5-7.

[Claim 9] The manufacture approach of the semiconductor integrated circuit equipment characterized by using the automatic wiring method in the manufacture approach of semiconductor integrated circuit equipment given in any 1 term of claims 5-8 in case said wiring layer of the 4th layer is arranged from said wiring layer of the 1st layer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to semiconductor integrated circuit equipment and its manufacturing technology.
[0002]
[Description of the Prior Art] As for semiconductor integrated circuit equipment, high integration and micro-processing-ization are promoted, in connection with it, wiring structure also becomes detailed and the wiring structure of high density has been required.
[0003] By the way, this invention person examined the manufacturing technology of semiconductor integrated circuit equipment. The following is the technique examined by this invention person, and the outline is as follows.
[0004] That is, as a wiring layer of semiconductor integrated circuit equipment, multilayer-interconnection structure is adopted and electrical connection of a lower layer wiring layer and the upper wiring layer is carried out through the connection hole (through hole) of the alternative field of an interlayer insulation film.
[0005] By the automatic wiring method which used CAD (Computer Aided Design) in wiring with a macro cell and a macro cell etc. in this case, it arranges so that a lower layer wiring layer and the upper wiring layer may be intersected perpendicularly.
[0006] In addition, as reference with which the formation technique of the wiring layer in semiconductor integrated circuit equipment is indicated, there will be some which are indicated by "'90 newest semi-conductor process technical" p267-p273 of Press Journal Issue Narimoto Taira year 11 month 2 day, for example.
[0007]
[Problem(s) to be Solved by the Invention] However, in the multilayer-interconnection structure of the mode arranged so that the lower layer wiring layer and the upper wiring layer which were mentioned above may be intersected perpendicularly, when carrying out the laminating of the multilayer wiring layers, such as four etc. layers, while it becomes complicated to carry out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film, the trouble that it is difficult to manufacture a highly efficient multilayer-interconnection layer has occurred.
[0008] The purpose of this invention is to offer the semiconductor integrated circuit equipment which has the multilayer-interconnection layer which can be manufactured highly efficiently and easily moreover, and its manufacturing technology.
[0009] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0010]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0011] Namely, the semiconductor integrated circuit equipment of this invention has the wiring layer of the 1st layer which lies at right angles, the wiring layer of a two-layer eye and the wiring layer of the 3rd layer which lies at right angles, and the wiring layer of the 4th layer. The wiring pitch of the wiring layer of the 1st layer and the wiring pitch of the wiring layer of a two-layer eye are equal. For the wiring pitch of the wiring layer of the 3rd layer, and the wiring pitch of the wiring layer of the 4th layer, it is equal and the wiring pitch of the wiring layer of the 3rd layer and the wiring layer of the 4th layer is 21/2 of the wiring pitches of the wiring layer of the 1st layer, and the wiring layer of a two-layer eye. It is twice.

[0012]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, what has the same function in the complete diagram for explaining the gestalt of operation attaches the same sign, and duplication explanation is omitted.
[0013] (Gestalt 1 of operation) Drawing 1 is the mimetic diagram showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[0014] In case this drawing carries out DA (Design Automation) processing of the arrangement of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, it is illustrating the channel and the lattice point of a wiring layer. In this case, the channel is setting line breadth of a wiring layer to 0, and shows the field of a wiring layer which can be arranged. Moreover, the lattice point shows the crossing of each channel.
[0015] The channel 1 for the 1st wiring layer corresponding to the wiring layer of the 1st layer arranged in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation on the semi-conductor substrate (illustration is omitted) with which two or more semiconductor devices are formed as shown in drawing 1 is the wiring pitch P1 with fixed spacing of the adjoining wiring layer. It is arranged in the longitudinal direction so that it may become.
[0016] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 2 for the 2nd wiring layer corresponding to the wiring layer of the two-layer eye arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of the 1st layer is arranged in the lengthwise direction so that it may intersect perpendicularly with the channel 1 for the 1st wiring layer, while it is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P1.
[0017] In this case, the lattice point which is a crossing of the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer is shown as the 1st lattice point 5.
[0018] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the 2nd lattice point 6 and the 3rd lattice point 7 are arranged at the midpoint of the 1st adjoining lattice point 5 in the channel 2 for the 2nd wiring layer.
[0019] In this case, the 2nd lattice point 6 and the 3rd lattice point 7 are arranged by turns so that each may serve as a hound's-tooth check.
[0020] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 3 for the 3rd wiring layer corresponding to the wiring layer of the 3rd layer arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of a two-layer eye is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P2. Moreover, the channel 3 for the 3rd wiring layer is arranged so that it may pass along the 2nd lattice point 6, while whenever [tilt-angle] is 45 degrees to the channel 2 for the 2nd wiring layer.
[0021] In this case, wiring pitch P2 of the channel 3 for the 3rd wiring layer Wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer Relation is P2 =21/2 xP1. It has become.
[0022] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the 4th lattice point 8 is arranged at the midpoint of the 1st adjoining lattice point 5 in the channel 1 for the 1st wiring layer.
[0023] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 4 for the 4th wiring layer corresponding to the wiring layer of the 4th layer

arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of the 3rd layer is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P2. Moreover, the channel 4 for the 4th wiring layer is arranged so that it may pass along the 4th lattice point 8, while whenever [tilt-angle] is 45 degrees to the channel 3 for the 3rd wiring layer.

[0024] In this case, wiring pitch P2 of the channel 4 for the 4th wiring layer Wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer Relation is P2 =21/2 xP1. It has become.

[0025] In the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, the channel 2 for the 2nd wiring layer lies at right angles to the channel 1 for the 1st wiring layer.

[0026] Moreover, as for the channel 3 for the 3rd wiring layer, whenever [tilt-angle] is arranged with 45 degrees to the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.

[0027] Moreover, while the channel 4 for the 4th wiring layer lies at right angles to the channel 3 for the 3rd wiring layer, whenever [tilt-angle] is arranged with 45 degrees to the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.

[0028] Moreover, wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer It is equal.

[0029] Moreover, wiring pitch P2 of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer It is equal.

[0030] And wiring pitch P2 of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer The relation with the wiring pitch P1 of the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer is P2 =21/2 xP1. It has become.

[0031] Therefore, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, when carrying out electrical connection of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 1st lattice point 5 which is a crossing of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.

[0032] Moreover, when carrying out electrical connection of the channel 2 for the 2nd wiring layer, and the channel 3 for the 3rd wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 2nd lattice point 6 which is a crossing of the channel 2 for the 2nd wiring layer, and the channel 3 for the 3rd wiring layer.

[0033] Moreover, when carrying out electrical connection of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 4th lattice point 8 which is a crossing of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer.

[0034] Therefore, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer like the channel 3 for the 3rd wiring layer and the channel 4 for the 4th wiring layer can be arranged according to a predetermined convention, the arranging method by the automatic wiring method using CAD can be used.

[0035] Consequently, by the ability using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.

[0036] Moreover, it sets to the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above. Since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer like the channel 3 for the 3rd wiring layer and the channel 4 for the 4th wiring layer can be arranged according to a predetermined convention For example, by the ability arranging each wiring layer with the minimum distance, while being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film in wiring with a macro cell and a macro cell etc. It can consider as highly efficient semiconductor

integrated circuit equipment.
[0037] Next, the manufacture approach of the wiring layer of the semiconductor integrated circuit equipment of the gestalt this operation is explained.
[0038] Drawing 2 - drawing 5 are the outline layout patterns showing the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation.
[0039] The manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is using the arranging method by the automatic wiring method for having used CAD.
[0040] First, as shown in drawing 2 , the wiring layer 9 of the 1st layer is formed on the semi-conductor substrate (illustration is omitted) with which two or more semiconductor devices are formed.
[0041] In this case, a wiring layer 9 is the wiring pitch P1 with fixed spacing of the adjoining wiring layer 9. It forms in a longitudinal direction so that it may become. Moreover, wiring pitch P1 Wiring width of face a1 of a wiring layer 9 Tooth-space width of face b1 between the adjoining wiring layers 9 It is considering as the applied distance.
[0042] Next, wiring pitch P1 with spacing of the wiring layer 10 which adjoins the wiring layer 10 of a two-layer eye through an interlayer insulation film (illustration is omitted) on the wiring layer 9 of the 1st layer fixed as shown in drawing 3 While forming so that it may become, it forms in a lengthwise direction so that it may intersect perpendicularly with the wiring layer 9 of the 1st layer.
[0043] In this case, wiring pitch P1 Wiring width of face a2 of a wiring layer 10 Tooth-space width of face b2 between the adjoining wiring layers 10 It is considering as the applied distance.
[0044] Moreover, the 1st connection hole 13 can be formed in the crossing of the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye if needed.
[0045] Next, wiring pitch P2 with spacing of the wiring layer 11 which adjoins the wiring layer 11 of the 3rd layer through an interlayer insulation film (illustration is omitted) on the wiring layer 10 of a two-layer eye fixed as shown in drawing 4 It forms so that it may become.
[0046] Moreover, the wiring layer 11 of the 3rd layer is formed so that it may pass along the 2nd lattice point 6 mentioned above while whenever [tilt-angle] had turned into 45 degrees to the wiring layer 10 of a two-layer eye.
[0047] In this case, wiring pitch P2 Wiring width of face a3 of a wiring layer 11 Tooth-space width of face b3 between the adjoining wiring layers 11 It is considering as the applied distance.
[0048] Moreover, the 2nd connection hole 14 can be formed in the crossing of the wiring layer 10 of a two-layer eye, and the wiring layer 11 of the 3rd layer if needed.
[0049] Next, wiring pitch P2 with spacing of the wiring layer 12 which adjoins the wiring layer 12 of the 4th layer through an interlayer insulation film (illustration is omitted) on the wiring layer 11 of the 3rd layer fixed as shown in drawing 5 While forming so that it may become, it forms so that it may intersect perpendicularly with the wiring layer 11 of the 3rd layer.
[0050] In this case, wiring pitch P2 Wiring width of face a4 of a wiring layer 12 Tooth-space width of face b4 between the adjoining wiring layers 12 It is considering as the applied distance.
[0051] Moreover, the 3rd connection hole 15 can be formed in the crossing of the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer if needed.
[0052] Next, after carrying out by repeating the production process of the wiring layer mentioned above if needed and forming a multilayer-interconnection layer, manufacture of semiconductor integrated circuit equipment is ended by forming a passivation membrane (illustration being omitted).
[0053] According to the manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above The arranging method by the automatic wiring method using CAD is used. Like the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer By the ability arranging the multilayer-interconnection layer which has the slanting wiring layer which inclines to the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye according to a predetermined convention Using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.
[0054] Moreover, according to the manufacturing technology of the wiring layer of the semiconductor

integrated circuit equipment of the gestalt of this operation mentioned above The arranging method by the automatic wiring method using CAD is used. Like the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer By the ability arranging the multilayer-interconnection layer which has the slanting wiring layer which inclines to the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye according to a predetermined convention While being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film, by the ability arranging each wiring layer with the minimum distance, highly efficient semiconductor integrated circuit equipment can be manufactured.

[0055] (Gestalt 2 of operation) Drawing 6 is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[0056] As shown in drawing 6 , the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation The wiring layer for connection holes currently embedded at the connection hole 16, the connection hole 17, and the connection hole 18 which are prepared between the wiring layer 11 of the 10 or 3rd layer of the wiring layer of a two-layer eye and the wiring layers 12 of the 4th layer, and those lower layer wiring layers For example, it is characterized by being the pillar (pillar) of the column configuration formed using connection hole embedding techniques, such as a plug.

[0057] Since the wiring layer for connection holes can be certainly embedded at the connection hole even if it is the connection hole of a high aspect ratio and is the case that the depth of a connection hole is large, by using the pillar of a column configuration as a wiring layer for connection holes, it is highly efficient and, moreover, can consider as a highly reliable wiring layer.

[0058] The channel and the lattice point in a wiring layer of semiconductor integrated circuit equipment of this operation are the same as the channel and the lattice point in the wiring layer of the semiconductor integrated circuit equipment of the gestalt 1 of operation mentioned above, and are as being shown in drawing 1 . [of a gestalt]

[0059] The wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is explained to a detail using drawing 1 and drawing 6 .

[0060] The manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is using the arranging method by the automatic wiring method for having used CAD.

[0061] The 3rd lattice point 7 shown in drawing 1 is also a crossing of the channel 2 for the 2nd wiring layer, and the channel 4 for the 4th wiring layer. The connection hole 16 which carries out electrical connection of the wiring layer 10 of a two-layer eye and the wiring layer 12 of the 4th layer which are shown in drawing 6 is arranged at this 3rd lattice point 7, and the wiring layer for connection holes is embedded at that connection hole 16.

[0062] The 4th lattice point 8 shown in drawing 1 is also a crossing of the channel 1 for the 1st wiring layer, and the channel 3 for the 3rd wiring layer. The connection hole 17 which carries out electrical connection of the wiring layer 9 of the 1st layer and the wiring layer 11 of the 3rd layer which are shown in drawing 6 is arranged at this 4th lattice point 8, and the wiring layer for connection holes is embedded at that connection hole 17.

[0063] In this case, the wiring layer 10 of a two-layer eye is partially isolated so that the wiring layer 10 of a two-layer eye may not adjoin, and even if the signal current is flowing to the wiring layer 10 of a two-layer eye, let the arrangement location of the connection hole 17 be the field which is electrically uninfluential.

[0064] Moreover, the connection hole 18 which carries out electrical connection of the wiring layer 9 of the 1st layer and the wiring layer 12 of the 4th layer which are shown in drawing 6 is arranged at the 4th lattice point 8 shown in drawing 1 , and the wiring layer for connection holes is embedded at the connection hole 18.

[0065] In this case, the wiring layer 10 of a two-layer eye is partially isolated so that the wiring layer 10 of a two-layer eye may not adjoin, and even if the signal current is flowing to the wiring layer 10 of a two-layer eye, let the arrangement location of the connection hole 18 be the field which is electrically uninfluential.

[0066] Moreover, the wiring layer 11 of the 3rd layer is partially isolated so that the wiring layer 11 of the 3rd layer may not adjoin, and even if the signal current is flowing to the wiring layer 11 of the 3rd layer, let the arrangement location of the connection hole 18 be the field which is electrically uninfluential.
[0067] Moreover, explanation is omitted according to arrangement of the connection hole for carrying out electrical connection of the adjoining lower layer wiring layer and the upper wiring layer being the same as arrangement of the connection hole in the wiring layer of the semiconductor integrated circuit equipment of the gestalt 1 of operation mentioned above.
[0068] According to the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, when it has a deep connection hole so that electrical connection can be carried out by the wiring layer for connection holes by which the wiring layer 10 of a two-layer eye and the wiring layer 12 of the 4th layer are embedded at the connection hole 16, electrical connection of a lower layer wiring layer and the upper wiring layer can be carried out by using the pillar of a column configuration as a wiring layer for connection holes.
[0069] Therefore, when carrying out electrical connection of a lower layer wiring layer and the upper wiring layer, the layout area of a multilayer-interconnection layer can be reduced by the ability making unnecessary the characteristic wiring layer for carrying out electrical connection of them.
[0070] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.
[0071] For example, various bases, such as a SOI (Silicon on Insulator) substrate, can be used instead of the semi-conductor substrate which forms a semiconductor device, and it can consider as semiconductor integrated circuit equipments, such as Processor LSI, and the manufacturing technology of those.
[0072]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0073] (1) In the wiring layer of the semiconductor integrated circuit equipment of . this invention, since the multilayer-interconnection layer which has the slanting wiring layer which inclines by whenever [tilt-angle / of about 45 degrees] to the channel for the 1st wiring layer and the channel for the 2nd wiring layer like the channel for the 3rd wiring layer and the channel for the 4th wiring layer can be arranged according to a predetermined convention, the arranging method by the automatic wiring method using CAD can be used.
[0074] Consequently, by the ability using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.
[0075] (2) In the wiring layer of the semiconductor integrated circuit equipment of . this invention like the channel for the 3rd wiring layer, and the channel for the 4th wiring layer Since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel for the 1st wiring layer and the channel for the 2nd wiring layer can be arranged according to a predetermined convention For example, by the ability arranging each wiring layer with the minimum distance, while being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film in wiring with a macro cell and a macro cell etc. It can consider as highly efficient semiconductor integrated circuit equipment.
[0076] (3) According to the wiring layer of the semiconductor integrated circuit equipment of . this invention, when it has a deep connection hole so that electrical connection can be carried out by the wiring layer for connection holes by which the wiring layer of a two-layer eye and the wiring layer of the 4th layer are embedded at the connection hole, electrical connection of a lower layer wiring layer and the upper wiring layer can be carried out by using the pillar of a column configuration as a wiring layer for connection holes.
[0077] Therefore, when carrying out electrical connection of a lower layer wiring layer and the upper wiring layer, the layout area of a multilayer-interconnection layer can be reduced by the ability making

unnecessary the characteristic wiring layer for carrying out electrical connection of them.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to semiconductor integrated circuit equipment and its manufacturing technology.

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PRIOR ART

[Description of the Prior Art] As for semiconductor integrated circuit equipment, high integration and micro-processing-ization are promoted, in connection with it, wiring structure also becomes detailed and the wiring structure of high density has been required.
[0003] By the way, this invention person examined the manufacturing technology of semiconductor integrated circuit equipment. The following is the technique examined by this invention person, and the outline is as follows.
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[0005] By the automatic wiring method which used CAD (Computer Aided Design) in wiring with a macro cell and a macro cell etc. in this case, it arranges so that a lower layer wiring layer and the upper wiring layer may be intersected perpendicularly.
[0006] In addition, as reference with which the formation technique of the wiring layer in semiconductor integrated circuit equipment is indicated, it is Narimoto Taira year 11 month 2 day and Press Journal Issue, for example.

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EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0073] (1) In the wiring layer of the semiconductor integrated circuit equipment of . this invention, since the multilayer-interconnection layer which has the slanting wiring layer which inclines by whenever [tilt-angle / of about 45 degrees] to the channel for the 1st wiring layer and the channel for the 2nd wiring layer like the channel for the 3rd wiring layer and the channel for the 4th wiring layer can be arranged according to a predetermined convention, the arranging method by the automatic wiring method using CAD can be used.
[0074] Consequently, by the ability using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.
[0075] (2) In the wiring layer of the semiconductor integrated circuit equipment of . this invention like the channel for the 3rd wiring layer, and the channel for the 4th wiring layer Since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel for the 1st wiring layer and the channel for the 2nd wiring layer can be arranged according to a predetermined convention For example, by the ability arranging each wiring layer with the minimum distance, while being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film in wiring with a macro cell and a macro cell etc. It can consider as highly efficient semiconductor integrated circuit equipment.
[0076] (3) According to the wiring layer of the semiconductor integrated circuit equipment of . this invention, when it has a deep connection hole so that electrical connection can be carried out by the wiring layer for connection holes by which the wiring layer of a two-layer eye and the wiring layer of the 4th layer are embedded at the connection hole, electrical connection of a lower layer wiring layer and the upper wiring layer can be carried out by using the pillar of a column configuration as a wiring layer for connection holes.
[0077] Therefore, when carrying out electrical connection of a lower layer wiring layer and the upper wiring layer, the layout area of a multilayer-interconnection layer can be reduced by the ability making unnecessary the characteristic wiring layer for carrying out electrical connection of them.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in the multilayer-interconnection structure of the mode arranged so that the lower layer wiring layer and the upper wiring layer which were mentioned above may be intersected perpendicularly, when carrying out the laminating of the multilayer wiring layers, such as four etc. layers, while it becomes complicated to carry out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film, the trouble that it is difficult to manufacture a highly efficient multilayer-interconnection layer has occurred.
[0008] The purpose of this invention is to offer the semiconductor integrated circuit equipment which has the multilayer-interconnection layer which can be manufactured highly efficiently and easily moreover, and its manufacturing technology.
[0009] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

[Translation done.]

* NOTICES *

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MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0011] Namely, the semiconductor integrated circuit equipment of this invention has the wiring layer of the 1st layer which lies at right angles, the wiring layer of a two-layer eye and the wiring layer of the 3rd layer which lies at right angles, and the wiring layer of the 4th layer. The wiring pitch of the wiring layer of the 1st layer and the wiring pitch of the wiring layer of a two-layer eye are equal. For the wiring pitch of the wiring layer of the 3rd layer, and the wiring pitch of the wiring layer of the 4th layer, it is equal and the wiring pitch of the wiring layer of the 3rd layer and the wiring layer of the 4th layer is 21/2 of the wiring pitches of the wiring layer of the 1st layer, and the wiring layer of a two-layer eye. It is twice.

[0012]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, what has the same function in the complete diagram for explaining the gestalt of operation attaches the same sign, and duplication explanation is omitted.
[0013] (Gestalt 1 of operation) Drawing 1 is the mimetic diagram showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[0014] In case this drawing carries out DA (Design Automation) processing of the arrangement of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, it is illustrating the channel and the lattice point of a wiring layer. In this case, the channel is setting line breadth of a wiring layer to 0, and shows the field of a wiring layer which can be arranged. Moreover, the lattice point shows the crossing of each channel.
[0015] The channel 1 for the 1st wiring layer corresponding to the wiring layer of the 1st layer arranged in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation on the semi-conductor substrate (illustration is omitted) with which two or more semiconductor devices are formed as shown in drawing 1 is the wiring pitch P1 with fixed spacing of the adjoining wiring layer. It is arranged in the longitudinal direction so that it may become.
[0016] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 2 for the 2nd wiring layer corresponding to the wiring layer of the two-layer eye arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of the 1st layer is arranged in the lengthwise direction so that it may intersect perpendicularly with the channel 1 for the 1st wiring layer, while it is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P1.
[0017] In this case, the lattice point which is a crossing of the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer is shown as the 1st lattice point 5.
[0018] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the 2nd lattice point 6 and the 3rd lattice point 7 are arranged at the midpoint of the 1st adjoining lattice point 5 in the channel 2 for the 2nd wiring layer.
[0019] In this case, the 2nd lattice point 6 and the 3rd lattice point 7 are arranged by turns so that each

may serve as a hound's-tooth check.
[0020] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 3 for the 3rd wiring layer corresponding to the wiring layer of the 3rd layer arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of a two-layer eye is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P2. Moreover, the channel 3 for the 3rd wiring layer is arranged so that it may pass along the 2nd lattice point 6, while whenever [tilt-angle] is 45 degrees to the channel 2 for the 2nd wiring layer.
[0021] In this case, wiring pitch P2 of the channel 3 for the 3rd wiring layer Wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer Relation is P2 =21/2 xP1. It has become.
[0022] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the 4th lattice point 8 is arranged at the midpoint of the 1st adjoining lattice point 5 in the channel 1 for the 1st wiring layer.
[0023] Moreover, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation, the channel 4 for the 4th wiring layer corresponding to the wiring layer of the 4th layer arranged through the interlayer insulation film (illustration is omitted) on the wiring layer of the 3rd layer is arranged so that spacing of the adjoining wiring layer may serve as the fixed wiring pitch P2. Moreover, the channel 4 for the 4th wiring layer is arranged so that it may pass along the 4th lattice point 8, while whenever [tilt-angle] is 45 degrees to the channel 3 for the 3rd wiring layer.
[0024] In this case, wiring pitch P2 of the channel 4 for the 4th wiring layer Wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer Relation is P2 =21/2 xP1. It has become.
[0025] In the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, the channel 2 for the 2nd wiring layer lies at right angles to the channel 1 for the 1st wiring layer.
[0026] Moreover, as for the channel 3 for the 3rd wiring layer, whenever [tilt-angle] is arranged with 45 degrees to the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.
[0027] Moreover, while the channel 4 for the 4th wiring layer lies at right angles to the channel 3 for the 3rd wiring layer, whenever [tilt-angle] is arranged with 45 degrees to the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.
[0028] Moreover, wiring pitch P1 of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer It is equal.
[0029] Moreover, wiring pitch P2 of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer It is equal.
[0030] And wiring pitch P2 of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer The relation with the wiring pitch P1 of the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer is P2 =21/2 xP1. It has become.
[0031] Therefore, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, when carrying out electrical connection of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 1st lattice point 5 which is a crossing of the channel 1 for the 1st wiring layer, and the channel 2 for the 2nd wiring layer.
[0032] Moreover, when carrying out electrical connection of the channel 2 for the 2nd wiring layer, and the channel 3 for the 3rd wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 2nd lattice point 6 which is a crossing of the channel 2 for the 2nd wiring layer, and the channel 3 for the 3rd wiring layer.
[0033] Moreover, when carrying out electrical connection of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer through the connection hole in an interlayer insulation film, it can carry out through the 4th lattice point 8 which is a crossing of the channel 3 for the 3rd wiring layer, and the channel 4 for the 4th wiring layer.
[0034] Therefore, in the wiring layer of the semiconductor integrated circuit equipment of the gestalt of

this operation mentioned above, since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer like the channel 3 for the 3rd wiring layer and the channel 4 for the 4th wiring layer can be arranged according to a predetermined convention, the arranging method by the automatic wiring method using CAD can be used.

[0035] Consequently, by the ability using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.

[0036] Moreover, it sets to the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above. Since the multilayer-interconnection layer which has the slanting wiring layer which inclines to the channel 1 for the 1st wiring layer and the channel 2 for the 2nd wiring layer like the channel 3 for the 3rd wiring layer and the channel 4 for the 4th wiring layer can be arranged according to a predetermined convention For example, by the ability arranging each wiring layer with the minimum distance, while being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film in wiring with a macro cell and a macro cell etc. It can consider as highly efficient semiconductor integrated circuit equipment.

[0037] Next, the manufacture approach of the wiring layer of the semiconductor integrated circuit equipment of the gestalt this operation is explained.

[0038] Drawing 2 - drawing 5 are the outline layout patterns showing the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation.

[0039] The manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is using the arranging method by the automatic wiring method for having used CAD.

[0040] First, as shown in drawing 2 , the wiring layer 9 of the 1st layer is formed on the semi-conductor substrate (illustration is omitted) with which two or more semiconductor devices are formed.

[0041] In this case, a wiring layer 9 is the wiring pitch P1 with fixed spacing of the adjoining wiring layer 9. It forms in a longitudinal direction so that it may become. Moreover, wiring pitch P1 Wiring width of face a1 of a wiring layer 9 Tooth-space width of face b1 between the adjoining wiring layers 9 It is considering as the applied distance.

[0042] Next, wiring pitch P1 with spacing of the wiring layer 10 which adjoins the wiring layer 10 of a two-layer eye through an interlayer insulation film (illustration is omitted) on the wiring layer 9 of the 1st layer fixed as shown in drawing 3 While forming so that it may become, it forms in a lengthwise direction so that it may intersect perpendicularly with the wiring layer 9 of the 1st layer.

[0043] In this case, wiring pitch P1 Wiring width of face a2 of a wiring layer 10 Tooth-space width of face b2 between the adjoining wiring layers 10 It is considering as the applied distance.

[0044] Moreover, the 1st connection hole 13 can be formed in the crossing of the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye if needed.

[0045] Next, wiring pitch P2 with spacing of the wiring layer 11 which adjoins the wiring layer 11 of the 3rd layer through an interlayer insulation film (illustration is omitted) on the wiring layer 10 of a two-layer eye fixed as shown in drawing 4 It forms so that it may become.

[0046] Moreover, the wiring layer 11 of the 3rd layer is formed so that it may pass along the 2nd lattice point 6 mentioned above while whenever [tilt-angle] had turned into 45 degrees to the wiring layer 10 of a two-layer eye.

[0047] In this case, wiring pitch P2 Wiring width of face a3 of a wiring layer 11 Tooth-space width of face b3 between the adjoining wiring layers 11 It is considering as the applied distance.

[0048] Moreover, the 2nd connection hole 14 can be formed in the crossing of the wiring layer 10 of a two-layer eye, and the wiring layer 11 of the 3rd layer if needed.

[0049] Next, wiring pitch P2 with spacing of the wiring layer 12 which adjoins the wiring layer 12 of the 4th layer through an interlayer insulation film (illustration is omitted) on the wiring layer 11 of the 3rd layer fixed as shown in drawing 5 While forming so that it may become, it forms so that it may intersect perpendicularly with the wiring layer 11 of the 3rd layer.

[0050] In this case, wiring pitch P2 Wiring width of face a4 of a wiring layer 12 Tooth-space width of face b4 between the adjoining wiring layers 12 It is considering as the applied distance.
[0051] Moreover, the 3rd connection hole 15 can be formed in the crossing of the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer if needed.
[0052] Next, after carrying out by repeating the production process of the wiring layer mentioned above if needed and forming a multilayer-interconnection layer, manufacture of semiconductor integrated circuit equipment is ended by forming a passivation membrane (illustration being omitted).
[0053] According to the manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above The arranging method by the automatic wiring method using CAD is used. Like the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer By the ability arranging the multilayer-interconnection layer which has the slanting wiring layer which inclines to the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye according to a predetermined convention Using the automated wiring arranging method, it is efficient and, moreover, a highly reliable wiring layout can be performed easily.
[0054] Moreover, according to the manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above The arranging method by the automatic wiring method using CAD is used. Like the wiring layer 11 of the 3rd layer, and the wiring layer 12 of the 4th layer By the ability arranging the multilayer-interconnection layer which has the slanting wiring layer which inclines to the wiring layer 9 of the 1st layer, and the wiring layer 10 of a two-layer eye according to a predetermined convention While being able to simplify carrying out electrical connection of those lower layer wiring layers and upper wiring layers through the connection hole in an interlayer insulation film, by the ability arranging each wiring layer with the minimum distance, highly efficient semiconductor integrated circuit equipment can be manufactured.
[0055] (Gestalt 2 of operation) Drawing 6 is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.
[0056] As shown in drawing 6 , the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation The wiring layer for connection holes currently embedded at the connection hole 16, the connection hole 17, and the connection hole 18 which are prepared between the wiring layer 11 of the 10 or 3rd layer of the wiring layer of a two-layer eye and the wiring layers 12 of the 4th layer, and those lower layer wiring layers For example, it is characterized by being the pillar (pillar) of the column configuration formed using connection hole embedding techniques, such as a plug.
[0057] Since the wiring layer for connection holes can be certainly embedded at the connection hole even if it is the connection hole of a high aspect ratio and is the case that the depth of a connection hole is large, by using the pillar of a column configuration as a wiring layer for connection holes, it is highly efficient and, moreover, can consider as a highly reliable wiring layer.
[0058] The channel and the lattice point in a wiring layer of semiconductor integrated circuit equipment of this operation are the same as the channel and the lattice point in the wiring layer of the semiconductor integrated circuit equipment of the gestalt 1 of operation mentioned above, and are as being shown in drawing 1 . [of a gestalt]
[0059] The wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is explained to a detail using drawing 1 and drawing 6 .
[0060] The manufacturing technology of the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation is using the arranging method by the automatic wiring method for having used CAD.
[0061] The 3rd lattice point 7 shown in drawing 1 is also a crossing of the channel 2 for the 2nd wiring layer, and the channel 4 for the 4th wiring layer. The connection hole 16 which carries out electrical connection of the wiring layer 10 of a two-layer eye and the wiring layer 12 of the 4th layer which are shown in drawing 6 is arranged at this 3rd lattice point 7, and the wiring layer for connection holes is embedded at that connection hole 16.
[0062] The 4th lattice point 8 shown in drawing 1 is also a crossing of the channel 1 for the 1st wiring layer, and the channel 3 for the 3rd wiring layer. The connection hole 17 which carries out electrical

connection of the wiring layer 9 of the 1st layer and the wiring layer 11 of the 3rd layer which are shown in drawing 6 is arranged at this 4th lattice point 8, and the wiring layer for connection holes is embedded at that connection hole 17.

[0063] In this case, the wiring layer 10 of a two-layer eye is partially isolated so that the wiring layer 10 of a two-layer eye may not adjoin, and even if the signal current is flowing to the wiring layer 10 of a two-layer eye, let the arrangement location of the connection hole 17 be the field which is electrically uninfluential.

[0064] Moreover, the connection hole 18 which carries out electrical connection of the wiring layer 9 of the 1st layer and the wiring layer 12 of the 4th layer which are shown in drawing 6 is arranged at the 4th lattice point 8 shown in drawing 1 , and the wiring layer for connection holes is embedded at the connection hole 18.

[0065] In this case, the wiring layer 10 of a two-layer eye is partially isolated so that the wiring layer 10 of a two-layer eye may not adjoin, and even if the signal current is flowing to the wiring layer 10 of a two-layer eye, let the arrangement location of the connection hole 18 be the field which is electrically uninfluential.

[0066] Moreover, the wiring layer 11 of the 3rd layer is partially isolated so that the wiring layer 11 of the 3rd layer may not adjoin, and even if the signal current is flowing to the wiring layer 11 of the 3rd layer, let the arrangement location of the connection hole 18 be the field which is electrically uninfluential.

[0067] Moreover, explanation is omitted according to arrangement of the connection hole for carrying out electrical connection of the adjoining lower layer wiring layer and the upper wiring layer being the same as arrangement of the connection hole in the wiring layer of the semiconductor integrated circuit equipment of the gestalt 1 of operation mentioned above.

[0068] According to the wiring layer of the semiconductor integrated circuit equipment of the gestalt of this operation mentioned above, when it has a deep connection hole so that electrical connection can be carried out by the wiring layer for connection holes by which the wiring layer 10 of a two-layer eye and the wiring layer 12 of the 4th layer are embedded at the connection hole 16, electrical connection of a lower layer wiring layer and the upper wiring layer can be carried out by using the pillar of a column configuration as a wiring layer for connection holes.

[0069] Therefore, when carrying out electrical connection of a lower layer wiring layer and the upper wiring layer, the layout area of a multilayer-interconnection layer can be reduced by the ability making unnecessary the characteristic wiring layer for carrying out electrical connection of them.

[0070] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0071] For example, various bases, such as a SOI (Silicon on Insulator) substrate, can be used instead of the semi-conductor substrate which forms a semiconductor device, and it can consider as semiconductor integrated circuit equipments, such as Processor LSI, and the manufacturing technology of those.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the mimetic diagram showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 2] It is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 3] It is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 4] It is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 5] It is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.
[Drawing 6] It is the outline layout pattern showing the wiring layer of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.
[Description of Notations]
1 Channel for 1st Wiring Layer
2 Channel for 2nd Wiring Layer
3 Channel for 3rd Wiring Layer
4 Channel for 4th Wiring Layer
5 1st Lattice Point
6 2nd Lattice Point
7 3rd Lattice Point
8 4th Lattice Point
9 Wiring Layer
10 Wiring Layer
11 Wiring Layer
12 Wiring Layer
13 1st Connection Hole
14 2nd Connection Hole
15 3rd Connection Hole
16 Connection Hole
17 Connection Hole
18 Connection Hole
a1 Wiring width of face
a2 Wiring width of face
a3 Wiring width of face
a4 Wiring width of face
b1 Tooth-space width of face
b2 Tooth-space width of face

b3 Tooth-space width of face
b4 Tooth-space width of face
P1 Wiring pitch
P2 Wiring pitch

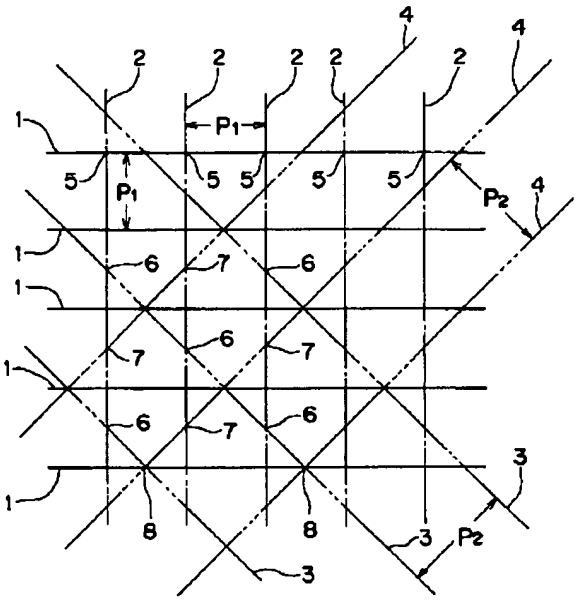
[Translation done.]

* NOTICES *

DRAWINGS

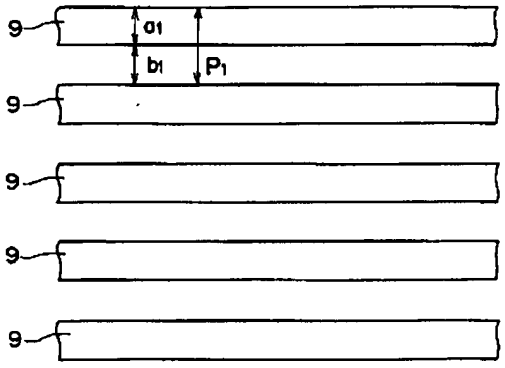
[Drawing 1]

図 1



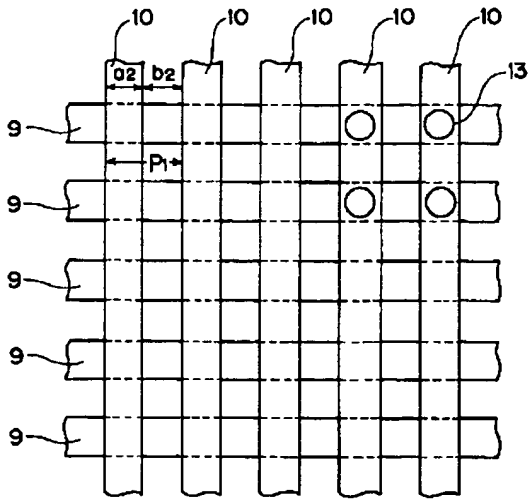
[Drawing 2]

図 2



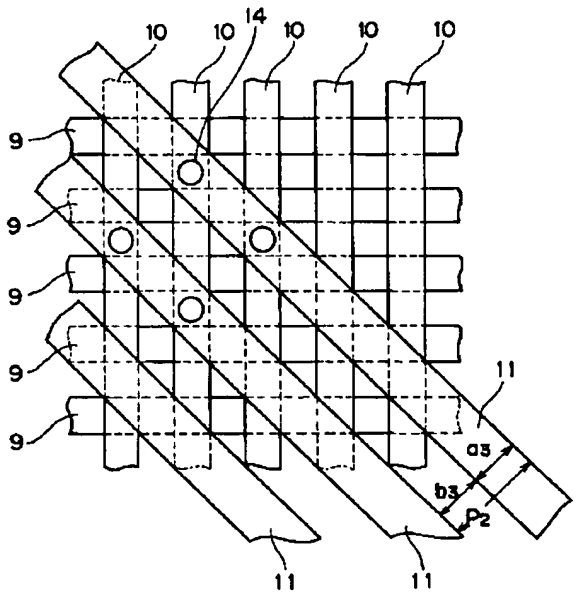
[Drawing 3]

図 3



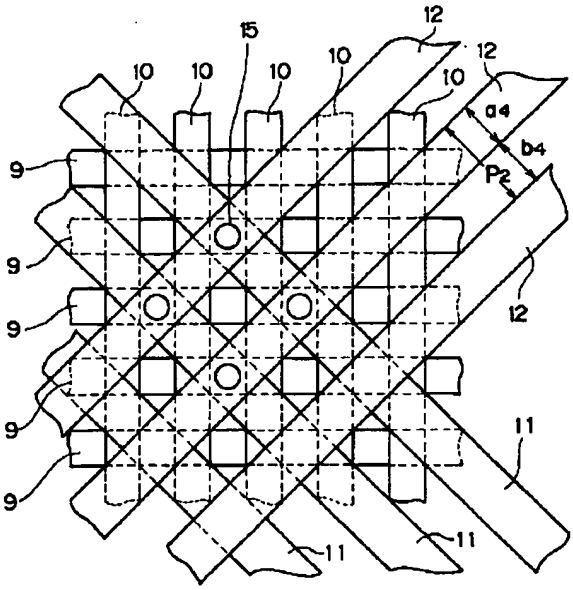
[Drawing 4]

図 4



[Drawing 5]

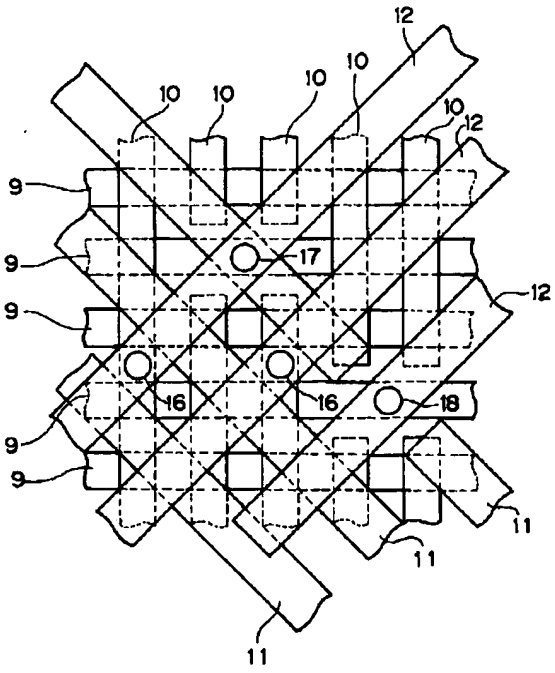
図 5



9：配線層　11：配線層
10：配線層　12：配線層

[Drawing 6]

図 6



[Translation done.]